

Form 1449\*

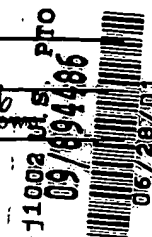
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INFORMATION DISCLOSURE STATEMENT  
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Applicant: Stephen R. Mooney et al.

Filing Date: Herewith

Group: 23/6  
Unknown

## U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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## FOREIGN PATENT DOCUMENTS

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## OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	
<i>Ge</i>	Donnelly, K.S., et al., "A 660MB/s Interface Megacell Portable Circuit in -.3 mum-0.7 mum CMOS ASIC", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 32, 1995-2003, (Dec. 1996)
<i>Ge</i>	Lee, T.H., et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 29, 1491-1496, (Dec. 1994)
<i>Ge</i>	Sidiropoulos, S., et al., "A Semidigital Dual Delay-Locked Loop", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 32, 1683-1692, (Nov. 1997)

Examiner

*Cassandra Cox*

Date Considered

*April 26, 2015*

\*Substitute Disclosure Statement Form (PTO-1449)

\*\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.